

REMARKS

Claims 1-15 are pending in this case. Based upon the following remarks, it is respectfully submitted that these claims are allowable.

A. §103 Rejection of Claims 1-15

Claims 1-15 remain rejected under 35 U.S.C. §103(a) as being unpatentable over Nishida et al., U.S. Patent No. 4,541,091 ("*Nishida et al.*"). This rejection is respectfully traversed and it is respectfully submitted that such a rejection cannot be based upon or supported by *Nishida et al.*

As expressly required in M.P.E.P. §2143, "[t]o establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." As the basis for the rejection, the Examiner has asserted that it would have been obvious to one having ordinary skill in the art at the time the invention was made to add RAM 28 after MODULATOR 32 in the circuit of Figure 4 of *Nishida et al.*, in conformance with M.P.E.P. §2143(I) ("There are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art."). However, "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." M.P.E.P. §2143(III). Further "[a] statement that modifications of the prior art to meet the claimed invention would have been 'well within the ordinary skill of the art at the time the claimed invention was made' because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references." M.P.E.P. §2143(IV). While it may be true that rearranging parts of an invention involves only routine skill in the art, the must still be a reason to do so. The Examiner has not cited, and it is

believed cannot cite, where or how *Nishida et al.* even suggests, much less teaches, some objective reason to rearrange its parts as described. In fact, contrary to M.P.E.P. §2143, which also states that “[t]he teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant’s disclosure” (emphasis added), the Examiner appears to infer a suggestion from the presently claimed invention.

Moreover, “[i]f [the] proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.” M.P.E.P. §2143(V). If RAM 28 was relocated to a position immediately following MODULATOR 32 in the circuit of Figure 4 of *Nishida et al.*, as suggested by the Examiner, the operation and functionality of the circuit of Figure 4 of *Nishida et al.* would be fundamentally altered and become “unsatisfactory for its intended purpose”. The signal generated by MODULATOR 32 is a PCM-modulated signal intended for microwave transmission, not for storage in RAM 28.

Moreover still, “[i]f the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious.” M.P.E.P. §2143(VI). Again, if RAM 28 was relocated to a position immediately following MODULATOR 32 in the circuit of Figure 4 of *Nishida et al.*, as suggested by the Examiner, the principle of operation of the circuit of Figure 4 of *Nishida et al.* would be fundamentally altered. Even if the PCM-modulated signal generated by MODULATOR 32 were suitable for storage in RAM 28, at a minimum, additional circuitry to support the use and function(s) of RAM 28 would be required, such as clocking or latching circuitry, or both, for writing data into and reading data out from RAM 28, as well as control circuitry for coordinating such additional functions, all of which are clearly beyond the scope of operation of that portion of the circuit of Figure 4 of *Nishida et al.*

Lastly, in the “Response to Amendment”, the Examiner states that “applicant’s claims do not recite that the storage unit should be at a specific location, it merely recites ‘storing said digital transmission signal,’ which is clearly taught by *Nishida et al.* and *Lovell et al.*” It is

respectfully submitted that, although a specific location per se may not be expressly recited, it is nonetheless clear that the storage unit must immediately follow the element performing the “modulating” since what is produced by such “modulating” is the “digital transmission signal” and it is that “digital transmission signal” which is stored. In other words, it is not some signal other than the “digital transmission signal” produced by the “modulating” that is stored in conformance with the recited limitation. Hence, contrary to the express requirements of the presently claimed invention, the Examiner has sought to equate various signals other than those produced by the modulator of *Nishida et al.* to the presently recited “digital transmission signal”.

B. §102 Rejection of Claims 1 & 12

Claims 1 and 12 remain rejected under 35 U.S.C. §102(e) as being anticipated by Lovell et al., U.S. Patent No. 6,831,945 ("*Lovell et al.*"). This rejection is respectfully traversed and it is submitted that these claims recite subject matter which is patentable over *Lovell et al.*

As noted in Amendment A, *Lovell et al.* was expressly described as lacking at least one of the presently recited elements. Accordingly, it is respectfully submitted that *Lovell et al.* cannot anticipate the presently claimed subject matter, and, therefore, rejection of these claims under 35 U.S.C. §102(e) is improper.

As further noted in Amendment A, immediately preceding this rejection in this same section was a reference to 35 U.S.C. §103(a), and further that, notwithstanding the fact that *Lovell et al.* lacks at least one of the presently recited elements, it was asserted that such element would have nonetheless been obvious to one of ordinary skill in the art. Therefore, in the event that this rejection is based upon 35 U.S.C. §103(a), it is respectfully submitted that such a rejection cannot be based upon or supported by *Lovell et al.*

As expressly required in M.P.E.P. §2143, “[t]o establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings.” As the basis for the rejection, the Examiner has asserted that it would have been obvious to one having ordinary skill

in the art at the time the invention was made to add RAM 28 after MODULATOR 32 in the circuit of Figure 4 of *Lovell et al.*, in conformance with M.P.E.P. §2143(I) (“There are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art.”). However, “[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.” M.P.E.P. §2143(III). Further “[a] statement that modifications of the prior art to meet the claimed invention would have been ‘well within the ordinary skill of the art at the time the claimed invention was made’ because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references.” M.P.E.P. §2143(IV). While it may be true that rearranging parts of an invention involves only routine skill in the art, the must still be a reason to do so. The Examiner has not cited, and it is believed cannot cite, where or how *Lovell et al.* even suggests, much less teaches, some objective reason to rearrange its parts as described. In fact, contrary to M.P.E.P. §2143, which also states that “[t]he teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant’s disclosure” (emphasis added), the Examiner appears to infer a suggestion from the presently claimed invention.

Moreover, “[i]f [the] proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.” M.P.E.P. §2143(V). If DIGITAL MODULATOR 5 was relocated to a position immediately preceding STORAGE BUFFER 7 in the circuit of Figure 4 of *Lovell et al.*, as suggested by the Examiner, the operation and functionality of the circuit of Figure 4 of *Lovell et al.* would be fundamentally altered and become “unsatisfactory for its intended purpose”. For example, in the circuitry in the right half of Figure 4, the signal generated by DIGITAL MODULATOR 5 is a signal intended for transmission via the upstream data path, not for storage in STORAGE BUFFER 7 in the downstream data path.

Moreover still, “[i]f the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious.” M.P.E.P. §2143(VI). Again, if DIGITAL MODULATOR 5 was relocated to a position immediately preceding STORAGE BUFFER 7 in the circuit of Figure 4 of *Lovell et al.*, as suggested by the Examiner, the principle of operation of the circuit of Figure 4 of *Lovell et al.* would be fundamentally altered. The signal provided by A/D CONVERTER 3 for storage in STORAGE BUFFER 7 already contains modulation introduced via a modulator upstream prior to its digital-to-analog conversion, downstream signal propagation and analog-to-digital conversion. The introduction of further modulation at this point, even if capable of maintaining some form of signal integrity, would produce a signal that would require further processing to recover the original data. Such further processing would be potentially significant and clearly unnecessary other than to simply undo the additional modulation introduced by the newly relocated DIGITAL MODULATOR 5, all of which are clearly beyond the scope of operation of that portion of the circuit of Figure 4 of *Lovell et al.*

Lastly, in the “Response to Amendment”, the Examiner states that “applicant’s claims do not recite that the storage unit should be at a specific location, it merely recites ‘storing said digital transmission signal,’ which is clearly taught by *Nishida et al.* and *Lovell et al.*” It is respectfully submitted that, although a specific location per se may not be expressly recited, it is nonetheless clear that the storage unit must immediately follow the element performing the “modulating” since what is produced by such “modulating” is the “digital transmission signal” and it is that “digital transmission signal” which is stored. In other words, it is not some signal other than the “digital transmission signal” produced by the “modulating” that is stored in conformance with the recited limitation. Hence, contrary to the express requirements of the presently claimed invention, the Examiner has sought to equate various signals other than those produced by the modulators of *Lovell et al.* to the presently recited “digital transmission signal”.

AMENDMENT B

C. Conclusion

Claims 1-15 remain pending in this case. Based upon the foregoing remarks, it is respectfully submitted that these claims are allowable, and reconsideration and early allowance of these claims are requested.

Respectfully submitted,

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